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EXAMINER	
TRINH, MICHAEL MANH	
ART UNIT	**PAPER NUMBER**
2822	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/551,187	ZENG, JUN	
	Examiner	Art Unit	
	Michael Trinh	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *76-93* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *76-93* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

*** This office action is in response to Applicant's amendment and RCE filed on June 13, 2005. Note that, in the claims of the amendment filed June 13, 2005, the phrase of "Claims 1-76 cancelled" is corrected as --Claims 1-75 cancelled--, since claim 76 is still existed and pending (37 CFR rule 126 for having consecutive claim number). Accordingly, Claims 1-75,94-104 were canceled. Claims 76-93 are pending.

*** The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

*** Claims 92-93 are objected to as claims 92-93 recite "the at least one device active region" while base claim 76 recites 'one or more device active regions". Correction is required.

*** Claim 76 is objected to, as the phrase "one or well" should be --one or more wells--. Correction is required.

Claim Rejections - 35 USC § 112

1. Claims 76-93 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

* In claim 76, in the step of --in the first surface, forming an one or more device action regions above the drain layer...", the term "the drain layer" lacks proper antecedent basis.

* In claims 77-79, the phrase "wherein the step of forming the pattern of recesses" is lacking proper antecedent basis, since base claim 76 does not recite any recesses ("forming a pattern of recesses..." in claim 76 was deleted by Applicant's amendment filed 6/13/05).

* In claims 81,83,84, the phrases "the recesses" (claim 81), "associated recess" (claim 83), and "at least one recess" (claim 84) are lacking proper antecedent basis and unclear, since base claim 76 does not recite any recess or recesses, and where the recess/recesses is/are located.

* In claims 86-87,88,89, the phrases "forming the recesses" (claims 86,87), "forming the at least one recess" (claim 88), and "forming the array of recesses" (claim 89) are lacking proper antecedent basis and unclear, since base claim 76 does not recite any recess or recesses, and where and when the recess is formed.

* Claim 77 is also indefinite as it depend on it-self of claim 77.

(Other dependent claims are also rejected as depending on rejected base claim)

Claim Rejections - 35 USC § 102

2. Claims 76,82-86,91-92 are rejected under 35 U.S.C. 102(e)/(a) as being anticipated by Okabe et al (5,663,096).

Re base claim 94, Obake teaches (at Figs 1-3; col 3, line 52 through col 5) a method for forming a semiconductor device comprising a semiconductor substrate having a first surface and second, opposite and planar surface and a lowered effective electrical resistivity, the method comprising: in the first surface, forming an one or more device active regions above the drain layer 2,1, said device active regions comprising one or more wells 4 of dopants of a second and opposite polarity and in said wells one or more source regions 6 of dopants of the first polarity the source regions laterally spaced from each other (Figs 1; col 3, line 52 through col 4); forming gate regions over portions of the well regions between the source regions and the drain layer; in the second, planar surface forming a highly doped drain region 1 (Fig 1; col 4, lines 1-18; cols 1-2; col 6, lines 1-36); and in the second, planar surface of the substrate after forming the highly doped drain region 1; forming one or more resistivity-lowering bodies 26 extending from the second, planar surface of the substrate into interior portions of the semiconductor substrate, wherein the resistivity-lowering bodies 26 formed in the concave recessed into the substrate comprises a material different than the semiconductor substrate 1 and having an electrical resistivity lower than an electrical resistivity of the semiconductor substrate (Figs 1,2B; col 4, line 20 through col 5, line 31), and having an electrical resistivity lower than an electrical resistivity of the semiconductor substrate 1, inherently (col 5, lines 57 through col 6, line 11) as the material comprises Ti-Ni-Au layers, wherein the Au layer is a contact layer. Re claim 82, wherein the electrode layer 26 including an electrical contact layer 26 and one or more of the resistivity-lowering bodies are formed on the second bottom surface of the semiconductor substrate. Re claim 83, wherein the resistivity-lowering body 26 is filled in the associated recess 22 (Figs 1,2B-2C). Re claim 84, wherein the electrode layer 26 includes a multilayer electrode so as to comprise a barrier layer lining in at least one recess (Fig 1,2C; col 6, lines 1-10). Re claim 85, wherein the resistivity lowering body of titanium, nickel, gold is inherently having an

electrical resistivity less than about 10^{-4} Ohms/cm (col 6, lines 1-11). Re claim 86, wherein as shown in figure 1, a proportion of the semiconductor substrate and the recesses is greater than about 0.4 percent. Re claims 91,92, MOSFET and IGBT are mentioned at col 6, lines 47-57. 76,82-86,91-92

Claim Rejections - 35 USC § 103

3. Claims 79-81,87,88-90,93 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okabe et al (5,663,096) taken with Iwai (4,597,166) and Yamane (JP-62243332).

Obake teaches a method (at Figs 1-3; col 3, line 52 through col 5) for forming a semiconductor device comprising a semiconductor substrate having a lowered effective electrical resistivity, as applied above to claims 76,82-86,91-92 and fully incorporated herein.

Obake teaches forming a plurality of recesses in the second bottom surface of the semiconductor substrate, but lack mentioning to form the recesses in grid pattern of cutting trenches, repeated pattern, trapezoidal pattern, array of recesses (79-81,88-90). Re claims 87 wherein the recess depth is greater than 25 percent of the semiconductor substrate.

However, Iwai teaches forming a plurality of recess into the second bottom surface of the semiconductor substrate, wherein the recesses comprising a repeated pattern, a grid pattern of cutting trenches, trapezoidal pattern, array of recesses (Figs 2A-7; col 4, line 40 through col 5). Yamane teaches grinding the second bottom surface oft eh semiconductor substrate 1 to form a plurality of recesses having a repeated pattern, a grid pattern of cutting trenches, and an array of recesses (Figs 1-3, English abstract). Re further claim 87, as shown in Iwai, the depth of the recesses is greater than 25 percent of the semiconductor substrate (Figs 2A-7).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the recesses of Okabe to have the recesses in repeated pattern, in grid pattern of cutting trenches, trapezoidal pattern, array of recesses, as taught by Iwai and Yamane. This is because of the desirability to form the recesses having diversity shapes including repeated pattern, in grid pattern of cutting trenches, trapezoidal pattern, array of recesses so that the electrode can be firmly adhered to the semiconductor substrate.

Re claim 93, although the references including Okabe does not mention a microprocessor used such semiconductor device, it is official notice that using such semiconductor device in forming a microprocessor is well known in the semiconductor art. Therefore, it would have been

obvious to one of ordinary skill in the art at least because of the desirability to form a computer having the micro processor for processing information and storing data since the semiconductor device is a low power consumption device.

4. Claims 76,79,82-87,91 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kubo (JP-62063472) taken with Pruniaux et al (3,823,352).

Kubo teaches forming a semiconductor device comprising a semiconductor substrate having a first surface and second, opposite and planar surface and a lowered effective electrical resistivity, the method (at Fig 1, English abstract) comprising: in the first surface, forming an one or more device active regions above the drain layer 2/1/12, said device active regions comprising one or more wells 3a-3c of dopants of a second and opposite polarity and in said wells one or more source regions 4a-4d of dopants of the first polarity the source regions laterally spaced from each other (Fig 1); forming gate regions 6a,6b over portions of the well regions between the source regions and the drain layer 2/1/12; in the second, planar surface forming a highly doped drain region 1; and in the second, planar surface of the substrate after forming the highly doped drain region 1; forming one or more resistivity-lowering bodies 10 extending from the second, planar surface of the substrate into interior portions of the semiconductor substrate, wherein the resistivity-lowering bodies formed in the concave recessed into the substrate comprises a conductive material different than the semiconductor substrate and having an electrical resistivity lower than an electrical resistivity of the semiconductor substrate, inherently. Re claim 79, wherein the pattern of recesses is repeated for a plurality of connected devices (Fig 1). Re claim 82, wherein the electrode layer 10 including an electrical contact layer and the resistivity-lowering bodies are formed in the recesses and on the second bottom surface of the semiconductor substrate (Fig 1). Re claim 84, wherein a barrier layer 10 or 12 is lining the recesses. Re claim 86, wherein as shown in figure 1, a proportion of the semiconductor substrate and the recesses is greater than about 0.4 percent. Re claim 87, wherein as shown in Figure 1, the recess extending into the substrate greater than about 25 percent. Re claim 91, wherein a MOSFET is mentioned at page 347, right column, last paragraph.

Re claims 76,83, Kubo teaches forming the electrode layer 10 in the recess, but appears lacking to have the resistivity-lowering bodies formed by filling the recesses. Re claim 85, wherein the resistivity of the resistivity lowering is less than about 10^{-4} Ohms/cm.

However, Pruniaux teaches (at Figs 1-3; col 4, line 1 through col 5) forming in the recess at least one lowering body 16 comprising a material having an electrical resistivity lower than that of the semiconductor substrate, wherein the material comprising platinum or platinum silicide, and forming a gold or silver contact layer by electroplating thereon (col 5, lines 40-47), wherein the resistivity lowering body of platinum, gold, silver is inherently having an electrical resistivity less than about 10^{-4} Ohms/cm.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the electrode of Kubo by filling the pattern of recesses with an electrical conductive metal as taught by Pruniaux. This is because of the desirability to provide effective thermal conduction, and to reduce substantially parasitic source resistance (in Pruniaux, col 5, lines 44-48; col 2, lines 9-15), wherein ON resistance of the device is reduced (English abstract of Kubo).

5. Claims 92-93 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kubo (JP-62063472) taken with Pruniaux et al (3,823,352), as applied to claims 76,79,82,83,85-87,91 above, and further of Okabe (5,663,096).

The references including Kubo and Pruniaux teach a method for forming a semiconductor device as applied to claims 76,79,82,83,85-87,91 above.

The references teach the device as a MOSFET, but lacks to mention to use the device in forming an IGBT (claim 92) or a microprocessor (claim 93).

However, Okabe et al teach (at col 6, lines 47-57) to apply the method in forming a device of MOSFET or IGBT.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the method in forming the device of MOSFET or IGBT as combinatively taught by Okabe and Pruniaux. This is because of the desirability to form high voltage devices having low ON-resistance. Re further claim 93, although the references including Okabe does not mention a microprocessor used such semiconductor device, it is official notice that using

such semiconductor device in forming a microprocessor is well known in the semiconductor art. Therefore, it would have been obvious to one of ordinary skill in the art at least because of the desirability to form a computer having the micro processor for processing information and storing data since the semiconductor device is a low power consumption device.

6. Claims 80-81,88-90 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kubo (JP-62063472) taken with Pruniaux et al (3,823,352), as applied to claims 76,79,82,83,85-87,91, above, and further of Iwai (4,597,166).

The references including Kubo and Pruniaux teach a method for forming a semiconductor device as applied to claims 76,79,82,83,85-87,91 above.

The references including Kubo and Pruniaux teach forming a plurality of recesses in the second bottom surface of the semiconductor substrate, but lack mentioning to form the recesses in grid pattern of cutting trenches, trapezoidal pattern, array of recesses (79-81,88-90).

However, Iwai teaches forming a plurality of recess into the second bottom surface of the semiconductor substrate, wherein the recesses comprising a repeated pattern, a grid pattern of cutting trenches, trapezoidal pattern, array of recesses (Figs 2A-7; col 4, line 40 through col 5).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the recesses of Kubo by forming the recesses in repeated pattern, in grid pattern of cutting trenches, trapezoidal pattern, array of recesses, as taught by Iwai, Kubo and Pruniaux. This is because of the desirability to form the recesses having various shapes including repeated pattern, in grid pattern of cutting trenches, trapezoidal pattern, array of recesses so that the electrode body can be formed into the recesses, thereby providing effective thermal conduction, and reducing substantially parasitic source resistance (in Pruniaux, col 5, lines 44-48; col 2, lines 9-15), wherein ON resistance of the device is thus reduced (English abstract of Kubo).

Response to Arguments

7. Applicant's remarks filed June 13, 2005 have been fully considered but they are not persuasive, and also moot in view of the new ground(s) of rejection.

Applicant remarked that "Claim 76 is amended to define the recesses...". However, there is no recess forming in claim 76. Claimed subject matter, not the specification, is the measure of invention. Limitations in the specification cannot be read into the claims for the purpose of avoiding the prior art. In Re Self, 213 USPQ 1,5 (CCPA 1982); In Re Priest, 199 USPQ 11,15 (CCPA 1978).

Applicant alleged that "The drain region is diffused from the second surface into the substrate and each point in any plane parallel to the second surface has the same concentration...". However, there is no diffusion in claim 76 from the second surface into the substrate and each point in any plane parallel to the second surface having the same concentration. Claimed subject matter, not the specification, is the measure of invention. Limitations in the specification cannot be read into the claims for the purpose of avoiding the prior art. In Re Self, 213 USPQ 1,5 (CCPA 1982); In Re Priest, 199 USPQ 11,15 (CCPA 1978). Moreover, the original specification must support for the claimed subject matter.

Applicant remarked about Kudo that the N+ layer 12 is formed after forming the grooves 11. However, Kudo also teaches forming the highly doped drain layer 1 before forming the grooves 11 (Figs 2 and 1).

** Cited of interested: Yamane shows an array of recesses formed by grinding and lapping, not randomly (Figs 1-3). Pelly (4,965,710) teaches using a semiconductor device in forming a microprocessor (abstract).

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Trinh whose telephone number is (571) 272-1847. The examiner can normally be reached on M-F from 8:30 Am to 4:30 Pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The central fax number is **(571) 273-8300.**

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Oacs-15

Michael Trinh
Primary Examiner